What is claimed is:

1. A power supply, comprising:

a power converter which converts input power to a DC power;

an output circuit which controls the DC power applied to a load in response to a drive voltage;

a digitally implemented slew rate controller which regulates a slew rate of a voltage of the DC power by changing a present value of the drive voltage supplied to the output circuit by incremental values at predetermined intervals to arrive at a final value of the drive voltage so that a maximum output current rating and a maximum output power rating of the output circuit are not exceeded at any value of the drive voltage while slewing the voltage of the DC power from the present value to the final value.

2. The power supply of claim 1, wherein the slew rate controller comprises:

a slope look-up table which stores the incremental values and which is indexed to be accessed according to the present value, the final value and a change direction of the drive voltage.

3. The power supply of claim 2, wherein the slew rate controller further comprises:

an input latch which latches the final value of the drive voltage input from an external source;

a first magnitude comparator which compares the final value with the present value to determine the change direction of the drive voltage;

an accumulator which sums the present value and one of the stored incremental values selected from the look-up table based on the present value, the final value and the direction of change of the drive voltage and outputs a next value of the drive voltage; and

an output latch which latches the next value as a new present value.

4. The power supply of claim 3, the slew rate controller further comprises:

a clipper which limits the next value to a predetermined maximum.

5. The power supply of claim 3, the slew rate controller further comprises:

a multiplexer which selects one of the next value and the final value and outputs the selected value to the output latch in response to a bypass control signal.

6. The power supply of claim 5, wherein:

the first magnitude comparator determines whether the final value equals the present value, the final value is greater than the present value or the final value is less than the present value; and

the slew rate controller further comprises:

a second magnitude comparator which compares the next value with the final value and determines whether the next value is less than the final value or greater than the final value, and

a bypass logic circuit which generates the bypass control signal so that the multiplexer selects the final value where the final value equals the present value, or the final value is greater than the present value and the next value is greater than the final value, or the final value is less than the present value and the next value is less than the final value.

7. The power supply of claim 6, wherein the bypass logic circuit generates the bypass control signal in response to an external command regardless of the values of the present value and the next value.

8. The power supply of claim 3, wherein the slew rate controller further comprises:

a slew latch which latches a value of a programmed slew value input from the external source;

a second magnitude comparator which compares the selected incremental value from the look-up table and the latched slew value; and

a multiplexer which provides the selected incremental value to the accumulator or replaces the selected incremental value with the latched slew value based on the comparison.

9. The power supply of claim 8, wherein, the multiplexer replaces the selected incremental value with the latched slew value if the latched slew value is less than the value selected from the slew rate table.

10. The power supply of claim 2, wherein each predetermined interval is an interval of a clock.

11. A digitally implemented slew rate controller for regulating a slew rate of a drive voltage of an electronic circuit, the slew rate controller comprising:

a slope look-up table which stores the incremental values and which is indexed to be accessed according to a present value, a final value and a change direction of the drive voltage.

an input latch which latches the final value of the drive voltage input from an external source;

a first magnitude comparator which compares the final value with the present value to determine the change direction of the drive voltage;

an accumulator which sums the present value and one of the stored incremental values selected from the look-up table based on the present value, the final value and the direction of change of the drive voltage and outputs a next value of the drive voltage; and

an output latch which latches the next value as a new present value.

12. The slew rate controller of claim 11, further comprising:

a clipper which limits the next value to a predetermined maximum.

13 The slew rate controller of claim 11, the slew rate controller further comprises:

a multiplexer which selects one of the next value and the final value and outputs the selected value to the output latch in response to a bypass control signal.

14. The slew rate controller of claim 13, wherein:

the first magnitude comparator determines whether the final value equals the present value, the final value is greater than the present value or the final value is less than the present value; and

the slew rate controller further comprises:

a second magnitude comparator which compares the next value with the final value and determines whether the next value is less than the final value or greater than the final value, and

a bypass logic circuit which generates the bypass control signal so that the multiplexer selects the final value where the final value equals the present value, or the final value is greater than the present value and the next value is greater than the final value, or the final value is less than the present value and the next value is less than the final value.

15. The slew rate controller of claim 14, wherein the bypass logic circuit generates the bypass control signal in response to an external command regardless of the values of the present value and the next value.

16. The slew rate controller of claim 11, wherein the slew rate controller further comprises:

a slew latch which latches a value of a programmed slew value input from the external source;

a second magnitude comparator which compares the selected incremental value from the look-up table and the latched slew value; and

a multiplexer which provides the selected incremental value to the accumulator or replaces the selected incremental value with the latched slew value based on the comparison.

17. The slew rate controller of claim 16, wherein, the multiplexer replaces the selected incremental value with the latched slew value if the latched slew value is less than the value selected from the slew rate table.

18. The slew rate controller of claim 11, wherein each predetermined interval is an interval of a clock.

19. A method of digitally controlling slew rate in a power supply, comprising:

providing a look-up table comprising values by which an output voltage of the power supply may be incremented without exceeding a maximum output current rating and a maximum output power rating of the power supply and which is indexed for accessing according to a present value, a final value and a direction of change of an output voltage of the power supply;

inputting a final value to which the output voltage is to be changed;

comparing the final value with the present value of the output voltage;

selecting one of the incremental values based on the present value, the final value and the direction of change of the output voltage;

summing the selected incremental value and the present value to obtain a next value;

latching the next value as a new present value;

stopping the incrementing of the output voltage based on comparing the next value with the final value and the comparing of the final value with the present value.

20. The method of claim 19, wherein the stopping of the incrementing comprises: stopping the incrementing where the final value equals the present value, or the final value is greater than the present value and the next value is greater than the final value, or the final value is less than the present value and the next value is less than the final value.